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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,595	10/03/2003	Brian W. Huber	DB000859-007	6161

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,595	HUBER, BRIAN W.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 July 2005 has been entered.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 15 July 2005. The changes and remarks disclosed therein have been considered.

No claims have been cancelled or added by the Amendment. Therefore, claims 1-9 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thaik (U.S. Pat. No. 5,285,116) in view of McClure (U.S. Pat. No. 5,619,456).

Regarding claims 1 and 6, Thaik in Figs. 4-7 discloses a pre-driver (24 and 26 in Fig. 4) providing an unbalanced output drive capability, comprising:

a first data path (24 in Fig. 4) for carrying a data signal (DRV-LOW-B), said first data path having a plurality of transistor output stages (including columns of transistors in Fig. 5A); a second data path (26 in Fig. 4) for carrying a data signal (DRV-HIGH), said second data path having a plurality of output stages (including columns of transistors in Fig. 6B);

and a plurality of switches (reasonably broadly interpreted as a unit that may include multiple transistors commonly controlled by a signal, such as N2 or N3 in Figs. 5A and 6B; similar to a double-pole, single-throw switch unit), each switch (for example, a switch comprising 51 and 102 commonly controlled by N2) for controlling (via, for example, N2) the conductivity of a pair (for example, the lower second columns of Figs. 5A and 6B) of the plurality of output stages in response to the level of conductivity of a subsequent driver output stage (or, to signals indicative of the strength of the output transistors in an output device) (for example, N2 is derived from an output buffer 20; see for example column 16, lines 4-6),

wherein one of said pair of output stages is connected to said first data path (for example, the lower second column of Fig. 5A within 24) and another of said pair of output stages is connected to said second data path (for example, the lower second column of Fig. 6B within 26).

However, Thaik does not disclose that the data signal for the second data path is a delayed version of said signal carried by said first data path.

McClure, for example in Figs. 2 and 6D, discloses a first data path for carrying a data signal (RBT 93) and a second data path for carrying a delayed version of said signal (RBC 91, which is an inverted version or a complement of RBT; i.e., a delayed version of RBT, delayed by

180 degrees). McClure further discloses a data output driver (comprising PFET 332 and NFET 334 in Fig. 6D) driven by the complementary pair of data lines (see 95 in Fig. 6D).

Since memories with a complementary pair of data lines and a data output driver driven by the complementary pair of data lines were common and well known in the art (as exemplified in McClure), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify and implement the output driver of Thaik in a memory with a complementary pair of data lines (such as that of McClure), such that the memory's existing complementary pair of data lines (i.e., one is a delayed version of the other) would be used for the pre-driver (in lieu of splitting a single data line, as in Thaik), for the purpose of improving the quality of data output signals in memories with complementary pair of data lines, by controlling the switching speed with maximum efficiency across process, temperature and supply voltage variations (Thaik, column 1, lines 6-13).

Regarding claims 7-9, the above combination of Thaik and McClure further discloses a computer system (see for example, Figs. 1, 2, 14 and 15 of McClure), comprising: a processor (within 560 in Fig. 14; 570 in Fig. 15; see also column 30, line 65 through column 31, line 13) having a processor bus (inherent, to communicate with peripheral devices); an input device (562) coupled to the processor through the processor bus; an output device (564) coupled to the processor through the processor bus; a memory device (50) coupled to the processor bus, the memory device comprising: a plurality of memory cells arranged in an array of rows and columns (Fig. 1); a plurality of devices for identifying cells within the array (including address decoders within 56 in Fig. 1; see also column 3, line 58 through column 4, line 5); a plurality of

pads (64); a data path connecting the plurality of pads and the array (see column 3, line 58 through column 4, line 5), the data path comprising an output driver (95 in Fig. 2) responsive to a data signal (RBT 93 or RBC 91).

Regarding claims 2-5, Thaik in Figs. 4-7 discloses a method of providing an unbalanced output drive capability to correct for output skews in subsequent amplification stages, comprising:

carrying a data signal (DRV-LOW-B) on a first data path (24) comprised of a plurality of output drive/pre-driver stages (for example, columns of transistors in Fig. 5A); carrying a data signal (DRV-HIGH) on a second data path (26) comprised of a plurality of output drive/pre-driver stages (for example, columns of transistors in Fig. 6B);

providing (for example, columns of transistors in Figs. 5A and 6B) on a first data path and on a second data path (24 and 26 in Fig. 4, respectively);

generating a two-bit code/signal (for example, N2 and N3) representative of the relative strength of an n-channel and a p-channel transistor in an output device (including 28, 30, 32, 34, and 36 in Fig. 4; see also, for example, column 16, lines 4-6 which discloses that the signals N2 and N3 are derived from an output buffer 20 in Fig. 4, which includes the output device);

controlling in pairs, or enabling, the number of output drive/pre-driver stages on said first and second data paths that are activated (for example, N2 and N3 activate in pairs the output stages in Figs. 5A and 6B) in response to the amount of skew represented by the two-bit code/signal (see, for example, column 5, lines 62-64), wherein at least a first pair (for example, the lower first columns of Figs. 5A and 6B) of said output stages is controlled by the first bit (for

example, N3) of said two-bit signal and at least a second pair (for example, the lower second columns of Figs. 5A and 6B) of said output stages is controlled by the second bit (for example, N2) of said two-bit signal, and wherein one output stage of each of said pairs is connected to said first data path (for example, the lower second column of Fig. 5A in 24) and another of each of said pairs of output stages is connected to said second data path (for example, the second column of Fig. 6B in 26), wherein said pre-driver produces an unbalanced output from the pre-driver (for example, the output DN1 in Fig. 5A; column 6, lines 36-38);

and inputting a data signal to the output device through the pre-driver (in Fig. 4, DATA SIGNAL is inputted to the output device through 24 and 26, which include Figs. 5A and 6B).

However, Thaik does not disclose that the data signal for the second data path is a delayed version of said signal carried by said first data path.

McClure, for example in Figs. 2 and 6D, discloses a first data path for carrying a data signal (RBT 93) and a second data path for carrying a delayed version of said signal (RBC 91, which is an inverted version or a complement of RBT; i.e., a delayed version of RBT, delayed by 180 degrees). McClure further discloses a data output driver (comprising PFET 332 and NFET 334 in Fig. 6D) driven by the complementary pair of data lines (see 95 in Fig. 6D).

Since memories with a complementary pair of data lines and a data output driver driven by the complementary pair of data lines were common and well known in the art (as exemplified in McClure), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify and implement the output driver of Thaik in a memory with a complementary pair of data lines (such as that of McClure), such that the memory's existing complementary pair of data lines (i.e., one is a delayed version of the other) would be used for

the pre-driver (in lieu of splitting a single data line, as in Thaik), for the purpose of improving the quality of data output signals in memories with complementary pair of data lines, by controlling the switching speed with maximum efficiency across process, temperature and supply voltage variations (Thaik, column 1, lines 6-13).

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,885,592 ("Reference") in view of McClure (U.S. Pat. No. 5,619,456).

Regarding claims 1-9, claims 1-13 of Reference recite a pre-driver, a method, a portion of data path, a memory device and a computer system as recited in claims 1-9, with the exception of the first pre-driver data path carrying a data signal and the second pre-drive data path carrying a delayed version of said data signal.

McClure, for example in Figs. 2 and 6D, discloses a first data path for carrying a data signal (RBT 93) and a second data path for carrying a delayed version of said signal (RBC 91,

which is an inverted version or a complement of RBT; i.e., a delayed version of RBT, delayed by 180 degrees). McClure further discloses a data output driver (comprising PFET 332 and NFET 334 in Fig. 6D) driven by the complementary pair of data lines (see 95 in Fig. 6D).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the second data path of Reference carry a delayed version (i.e., the complement) of the data signal, since memories with a complementary pair of data lines and a data output driver driven by the complementary pair of data lines were common and well known in the art (as exemplified in McClure).

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection, necessitated by the amendments.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/28/05

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh